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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P8123
First Inventor or Application Identifier	Brian Doyle
Title	QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME
Express Mail Label No.	EL414970584US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

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1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [*Total Pages 29*]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [*Total Sheets 8*]

4. Oath or Declaration [*Total Pages 3*]
a. ☐ Newly executed (original copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
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ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
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UNITED STATES LETTERS PATENT APPLICATION

FOR

QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME

DO NOT SCAN

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to integrated circuit fabrication, and, more specifically, the present invention relates to the fabrication of quantum wire gate structures that are spacer-width patterned.

Description of Related Art

During the tunneling of an electron from a source to a drain in a typical semiconductive transaction, an electron will suffer a number of collisions between source and drain that cause the electron path length to increase. Because electron flow is constant velocity, the longer electron path hinders the effective transition time thereof. With the advent of quantum wire devices, an electron is allowed only to suffer collisions that will be confined within the extremely narrow channel, including collisions at the interface between channel and contiguous dielectric. Thus, where the narrow channel has a width the is less than the mean free path (MFP) of the electron, conservation of momentum law dictates a more direct route through the channel and a faster transition time from source to drain.

A field effect transistor (FET) is a fundamental building block of integrated circuits. Where metal oxide on silicon (MOS) devices are approaching the limits of scaling based upon known fundamental technique, optimization of different components has allowed the FET to continue in the process of miniaturization. The decrease in supply voltage, however, has caused acceptable performance in the 0.7X scaling to become increasingly elusive. What is needed is a method of achieving gate dimensions that overcome scaling limits of the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention that are not necessarily drawn to scale and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1a is an elevational cross-section fractional view that depicts preliminary fabrication of a first layer for a quantum wire, double gate device;

Figure 1b is an elevational cross-section fractional view of the device depicted in Figure 1a after further processing;

Figure 1c illustrates further processing of the device in Figure 1b in which a spacer etch has been accomplished;

Figure 1d illustrates further processing wherein a first layer has been removed to leave a spacer mask;

Figure 1e illustrates further processing wherein a quantum wire has been formed in a semiconductive substrate;

Figure 1f illustrates further processing of the device depicted in Figure 1e, wherein the quantum wire has been overlaid with a gate layer;

Figure 2a is an elevational cross-section view of a substrate with a patterned oxide disposed thereon that has been precisely spaced apart;

Figure 2b is an elevational cross-section view that depicts further processing of the structure depicted in Figure 2a, wherein a nitride layer has been formed over the substrate and patterned oxide;

Figure 2c depicts further processing, wherein a spacer etch has left uniformly spaced-apart first nitride spacer masks;

Figure 2d depicts further processing after removal of the patterned oxide layer, followed by formation of a second oxide layer;

Figure 2e depicts further processing, wherein a spacer etch has formed uniformly-spaced-apart oxide spacer masks;

Figure 2f illustrates further processing, wherein the first nitride spacers have been removed;

Figure 2g illustrates further processing, wherein a second nitride layer has been formed and spacer etched;

Figure 2h illustrates further processing, wherein the oxide spacer masks have been removed to leave a plurality of uniformly spaced-apart second nitride spacer masks;

Figure 2i illustrates further processing, wherein quantum wires have been formed beneath the second nitride spacer masks by etching into the substrate;

Figure 3a is an elevational cross-section fractional view of a semiconductor structure that depicts another embodiment of the present invention;

Figure 3b depicts further processing of the structure depicted in Figure 3a;

Figure 3c depicts further processing of the structure depicted in Figure 3b;

Figure 4 is an elevational cross-section fractional view of an inventive quantum wire gate;

Figure 5 is an elevational cross-section fractional view of an inventive quantum wire gate;

Figure 6 is an elevational cross-section fractional view of an inventive quantum wire gate;

Figure 7 is an elevational cross-section fractional view of an inventive quantum wire gate;

Figure 8 is an elevational cross-section fractional view of an inventive quantum wire gate;

Figure 9 is an elevational perspective view of an inventive quantum wire gate; and

Figure 10 is a block diagram that illustrates process flow.

DETAILED DESCRIPTION OF THE INVENTION

The following description includes terms, such as upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. The embodiments of an apparatus or article of the present invention described herein can be manufactured, used, or shipped in a number of positions and orientations.

Reference will now be made to the drawings wherein like structures will be provided with like reference designations. In order to show the structures of the present invention most clearly, the drawings included herein are diagrammatic representations of integrated circuit structures. Thus, the actual appearance of the fabricated structures, for example in a photomicrograph, may appear different while still incorporating the essential structures of the present invention. Moreover, the drawings show only the structures necessary to understand the present invention. Additional structures known in the art have not been included to maintain the clarity of the drawings.

Figure 1a is an elevational cross-section fractional view of a larger structure that depicts preliminary fabrication of a quantum wire, spacer double gate device, depicted herein by reference numeral 10. Device 10 is fabricated by providing a substrate 12 and by patterning a first oxide 14 upon substrate 12. First oxide 14 has a characteristic width and a characteristic pitch. **Figure 1b** illustrates formation of a first nitride layer 16 over first oxide 14 and substrate 12. First nitride layer 16 has a thickness in a range from about 5 nm to about 20nm, preferably about 10 nm. First nitride layer 16 may be deposited by chemical vapor deposition (CVD), by physical vapor deposition (PVD), by nitridation of a PVD or CVD metal layer, or by other known methods. One method of forming first nitride layer 16 is to directly form a nitride layer upon substrate 12 and first oxide 14 by CVD or PVD of a nitride such as a metal nitride.

Preferably, first nitride layer 16 is formed by CVD of a refractory metal nitride such as silicon nitride.

Another method of forming first nitride layer 16 is to directly form a nitride layer upon substrate 12 and first oxide 14 by CVD or PVD of a nitride such as a refractory metal nitride. The metal nitride may be selected from any suitable metal according to a preferred usage. First nitride layer 16 may be formed by CVD of a refractory metal nitride such as titanium nitride.

A spacer etch is performed upon device 10 as depicted in **Figure 1c** to form a patterned first nitride spacer mask 18. Spacer etching is carried out by anisotropic etching, preferably by reactive ion etching (RIE). The RIE has an etch recipe that is selective to substrate 12 and to first oxide 14 over first nitride layer 16. The etch recipe may have a selectivity above about 2:1, preferably above about 10:1.

After the formation of first nitride spacer mask 18, first oxide layer 14 is removed by an etch that is selective to substrate 12 and to first nitride spacer mask 18. The result of this etch is depicted in **Figure 1d**. Preferably, the etch is a wet etch as is known in the art. Preferably selectivity of the etch recipe of oxide 14 and substrate 12-to- first nitride spacer mask 18 in range from about 2:1 to about 10:1 or greater.

Figure 1e illustrates further processing of structure 10. An anisotropic etch has been carried out on substrate 12 with the use of first nitride spacer mask 18. Etching into substrate 12 is carried out under conditions that will allow the formation of a quantum wire 20. Quantum wire 20 has the property of having a width W, defined by the thickness of layer 16, that is smaller than the mean free path of electrons that flow therein under semiconductive conditions. Quantum wire 20 may be an integral part of substrate. Even though doping of substrate 12 and of quantum wire 20 may be identical, due to the multiple gate structure and/or the proximity of

semiconductive channels in a double gate configuration, a semiconductive transaction occurs only in quantum wire 20. This phenomenon will be set forth below.

Figure 1f illustrates further processing of structure 10 depicted in Figure 1e, wherein quantum wire 20 has been overlaid with a gate layer 22. Gate layer 22 is preferably a metal-like material such as heavily p- or n-doped (e.g. about 1 X $10^{20}/cm^3$) or undoped polycrystalline silicon. It may also be a metal. In a preferred embodiment gate layer 22 may be formed by CVD followed by planarization such as by chemical-mechanical polishing (CMP). In this embodiment, quantum wire 20 forms a first semiconductive channel that is spaced apart from a second semiconductive channel 20 by a trench 32 that is greater than the channel width, preferably less than about five times the semiconductive channel width.

In some embodiments of the present invention, it is preferable to achieve a series of closely-spaced quantum wires in order to allow a contact to make electrical connection a maximum number of quantum wires, relative to the characteristic width of the contact. Where a contact has reached a cross-sectional area limit in the range from about 150 nm to about 250 nm, a maximum number of quantum wires can be formed beneath a contact that will facilitate a drive current such as a bit line communication through the quantum wires.

In accordance with the present invention, a method of forming a device with uniform and closely spaced quantum wires is provided. **Figure 2a** is an elevational cross-section view of a structure 200 that includes a substrate 12 with a patterned first oxide 14 disposed thereon. Patterned first oxide 14 is precisely spaced apart to allow crowding of quantum wires into a minimum area. In one embodiment, patterned first oxide 14 has a characteristic width, W, in a range from about 50 nm to about 200 nm, preferably about 100 nm. Patterned first oxide has a characteristic pitch, P, in a range from about 150 nm to about 600 nm, preferably about 300 nm.

Figure 2b is an elevational cross-section view that depicts further processing of structure 200 depicted in Figure 2a, wherein a first nitride layer 16 has been formed over substrate 12 and patterned first oxide 14. First nitride layer 16 may be any nitride layer suitable for a given application, and as set forth herein. First nitride layer 16 is preferably formed at a characteristic thickness that will result in a spacer width that is about an integer fraction of characteristic width W. For example, where W is about 100 nm, first nitride layer 16 is formed at a characteristic thickness of about 50 nm.

Figure 2c depicts further processing of structure 200 depicted in Figure 2b, wherein a spacer etch has left uniformly spaced-apart first nitride spacer masks 18 upon patterned first oxide layer 14. Removal of patterned first oxide layer 14 is next carried out by an etch that is selective to substrate 12 and to first nitride spacer masks 18. Etching to remove patterned first oxide layer 14 is carried out as set forth herein. Where W is about 100 nm, and first nitride layer 16 has a characteristic thickness of about 50 nm, uniformly spaced-apart first nitride spacer mask 18 may have a width of about 50 nm.

Figure 2d depicts further processing of structure 200 depicted in Figure 2c after removal of patterned first oxide layer 14. In Figure 2d, a second oxide layer 24 is formed over first nitride spacer mask 18. In this embodiment, second oxide layer 24 has a characteristic thickness of about 25 nm. A spacer etch is next performed upon the second oxide layer 24 as illustrated in **Figure 2e** to form uniformly-spaced first oxide spacer masks 26. The etch type and etch recipe selectivites are used as set forth herein.

Figure 2f illustrates further processing, wherein first nitride spacers 18 have been removed. First nitride spacer mask 18 is removed by an etch that may typically be wet. Preferably, the etch recipe will be selective to first oxide spacer mask 26 and to substrate 12.

Figure 2g illustrates further processing, wherein a second nitride layer has been formed and spacer etched to form a second nitride spacer mask 28. In this embodiment, the second nitride layer is about 10 nm thick and consequently, second nitride spacer mask 28 is about 10 nm wide. **Figure 2h** illustrates further processing. Thereby, first oxide spacer mask 26 is removed by a wet etch or the like and with an etch recipe that is selective to second nitride spacer mask 28 and to substrate 12.

Figure 2i illustrates further processing, wherein quantum wires 20 have been formed by etching into substrate 12. Where the characteristic width, W, was about 100 nm and the characteristic pitch, P, was about 300 nm, structure 10 has a plurality of quantum wires 20 that have a width 30 of about 10 nm. Additionally, quantum wires 20 are uniformly spaced apart by a trench 32 that has a trench width 34 of about 20 nm.

Other uniform spacing schemes may be accomplished according to the present invention. In one embodiment, W is about 100 nm and P is about 320 nm. By conducting the inventive method of this embodiment similar to the inventive method depicted in Figures 2a through 2i, trench width 34 and wire width 30 are of about equal length; in this embodiment each is about 10 nm.

Other dimensions of quantum wire 20 and of second nitride spacer mask 28 include the quantum wire height 36 and the second nitride spacer mask height 38. Preferably, quantum wire 20 is at least square in cross-sectional shape. Optionally, quantum wire 20 may have an aspect ratio of height 36-to-width 30 in a range from about 1.1 to about 5. Second nitride spacer mask 28 may be of any aspect ratio that is suited or incidental to a preferred fabrication scheme. Examples of the aspect ratio range include from about 0.2 to about 10. Preferably, second nitride

spacer mask 28 has an aspect ratio of about 1 or greater. Structure 200 depicted in Figure 2i may be further processed as set forth herein to form a quantum wire gate device.

Another uniform spacing scheme may be accomplished according to the present invention as illustrated in **Figure 3a**. In this embodiment, a structure such as second nitride spacer mask 28 is overlaid with a material such as an oxide layer 82. In **Figure 3b**, oxide layer 82 has been planarized back to about the top of second nitride spacer mask 28 to form an oxide block 84. With oxide block 84 in place, a directional etch may be carried out to create a quantum wire 320 and a trench 32 that spaces apart two quantum wires 320. By conducting the inventive method of this embodiment similar to the inventive method depicted in Figures 2, trench 32 has a width that is less than the quantum wire width.

Figure 4 is an elevational cross-section fractional view of an inventive quantum wire double gate 400. A double-gate quantum wire 420 comprises two semiconductive channels 42, 44 that are depicted by estimation phantom lines to delineate semiconductive transaction areas. As a whole, double-gate quantum wire 420 may be considered a semiconductive channel comprising a channel length and a channel width W. The channel length is orthogonal to the plane of the Figure. A dielectric layer such as a gate oxide layer 40 may be formed upon the semiconductive channel length as well as upon substrate 12. A gate layer 422 is disposed over the double-gate quantum wire 420.

Figure 5 is an elevational cross-section fractional view of an inventive quantum wire triple gate 500. A triple-gate quantum wire 520 comprises three semiconductive channels 42, 44, and 46 that are depicted by estimation with phantom lines to delineate semiconductive transaction areas. As a whole, triple-gate quantum wire 520 may be considered a semiconductive channel comprising a channel length and a channel width W. The channel

length is orthogonal to the plane of the Figure. A dielectric layer such as a gate oxide layer 40 may be formed upon the semiconductive channel length and width as well as upon substrate 12. Quantum wire triple gate 500 comprises three semiconductive channels 42, 44, and 46. A gate layer 522 is disposed over the double-gate quantum wire 520.

Figure 6 is an elevational cross-section fractional view of an inventive quantum wire single gate 600. A single-gate quantum wire 620 comprises a single semiconductive channel 46 that is depicted by estimation with phantom lines to delineate a semiconductive transaction area. As a whole, single-gate quantum wire 620 may be considered a semiconductive channel comprising a channel length and a channel width W. The channel length is orthogonal to the plane of the Figure. A bulk dielectric layer 48 covers quantum wire 620 and fills trench 32 to a level above quantum wire 620 that allows for semiconductive activity in channel 46. A gate layer 622 is disposed over the double-gate quantum wire 620.

Figure 7 depicts an inventive quantum wire, double gate structure 700 that is formed upon an insulator substrate 50. Some embodiments may preferably be a silicon on insulator (SOI) structure. An SOI structure completely isolates the quantum wire from any electrically conductive or semiconductive material such as where the substrate is a monocrystalline silicon. Typically in the structures depicted in Figures 1-6, semiconducting activity is limited to areas that are proximate the gate within the quantum wire. This limited semiconducting activity is either due to no other gate material being close enough to cause a field effect, or due to the collective effect of a first semiconductive area 42 being affected by electrical activity in a second semiconductive area 44 such as depicted in Figure 4. In other words, semiconductive activity in one area of a quantum wire synergistically promotes the semiconductive activity of another area therewithin.

Because the channel interface with dielectric material of the multiple gate structure decreases compared to a conventional gate, the charge current may more than double. It is discovered that at a 10 nm wire width, the charge current can be greater than about twice that of a single gate channel instead of the expected doubled charge current. In one test series, double gate structures showed an increase in charge current over a single-gate structure. The results of the tests were about 2.2 times the charge current, about 2.35 times, about 2.47 times, and about 2.49 times.

Figure 7 illustrates an SOI structure 700 that includes insulator substrate 50 that forms the SOI precursor set upon silicon 52. Therefrom, quantum wires 720 have been formed beneath a spacer mask such as second nitride spacer mask 28. In this embodiment, quantum wire 720 has been totally isolated from other electrically conductive or semiconductive material. A gate layer 722 is disposed over the double-gate quantum wire 720. It is understood that the SOI scheme may be applied in any of the embodiments set forth herein.

Figure 8 represents an embodiment in which ion implantation is carried out to create doping regions 54 that are self-aligned beneath trenches 32 that lie between second nitride spacer masks 28. This structure 800 has an electrical isolation effect that is similar to an SOI structure. For example, where substrate 12 is n-doped, self-aligned doping region 54 is heavily n-doped such that n-type semiconductivity is hindered therein. In such a doping scheme, it is preferable to employ doping elements that are more resistive to diffusion during subsequent processing including burn-in. In an n-type doped substrate, self-aligned doping region 54 may be doped with arsenic and the like. Preferably, the dopant will resist thermal diffusion compared to other dopant elements of the same type. Doping regions 54 resist electrical communication between two adjacent quantum wires 820.

It now become apparent that combination of an SOI with a self-aligned doping region may be carried out. In this embodiment, an SOI quantum wire is constructed that does not achieve complete isolation of the wires from their silicon substrate. In other words, etching does not proceed to the extent that the etch stops on the insulator; it stops short of this etch depth. Isolation is approximated, however, by the implantation of a doping region as set forth above. The doping region may extend to the insulator substrate, or it may only extend to a depth that causes the quantum wires to be effectively isolated from their monocrystalline silicon substrate. In this embodiment, the plurality of quantum wires maintains a structural integrity with their monocrystalline silicon substrate, but they are effectively isolated from each other as well as from the substrate. This embodiment may be achieved by forming a structure such as structure 800 as depicted in Figure 8, upon an insulator substrate such as insulator substrate 50, ass depicted in Figure 7.

Figure 9 is an elevational perspective view of an inventive quantum wire gate structure 900. A quantum wire 920 is disposed upon an insulator substrate 50. Quantum wire 920 has been patterned with the use of a spacer mask such as second nitride spacer mask 28. A gate layer 922 is disposed over quantum wire 920 and second nitride spacer mask 28 to create a quantum wire double gate in this embodiment. A gate oxide (not pictured) is formed upon the length 56 of quantum wire 920. An insulator 58 may also be formed. Additionally, where quantum wire 920 is to connect with a contact in a contact corridor, a gate spacer is to be formed between a contact landing area 60 and gate layer 22 by the traditional method of nitride/oxide deposition and an RIE spacer etch.

Figure 10 is a process flow diagram that illustrates the inventive method of forming a quantum wire gate. The process 1000 begins at block 1010 with patterning a first oxide upon a

substrate. At block 1020 the process continues by forming a first nitride spacer mask upon the first oxide. Next, a first oxide spacer mask is formed at block 1030. The first oxide spacer mask is formed upon the first nitride spacer mask. The process continues at block 1040 by forming a second nitride spacer mask upon the first oxide spacer mask. At block 1050, a plurality of channels is formed in the substrate. The plurality of channels are aligned to the second nitride spacer mask. At block 1060, a gate layer is formed over the plurality of channels. According to the present invention, each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.

Distinct advantages exist for the present invention. Because of the scale that has been achieved, the coupling effect of the a first channel gate upon the channel gate opposite thereto in the same quantum wire is synergistically enhanced even with lower gate potentials than are required by the smaller dimensions.

Another advantage exists where the same potential is felt across the gate by electrons that flow within each gate. Thus the potential of electrons in one gate affects the potential of electrons in the counterpart section of the double gate or the triple gate. Consequently, electrons tend to move more toward the middle of the quantum wire and mobility increases because electron flow near a dielectric interface is reduced. The inventive device therefore has about twice the drive current from what is expected. In other words the drive current, instead of being twice the drive current of a single gate device, tends to be closer to about four times the expected drive current for a single gate device.

It will be readily understood to those skilled in the art that various other changes in the details, material, and arrangements of the parts and method stages which have been described

and illustrated in order to explain the nature of this invention may be made without departing from the principles and scope of the invention as expressed in the subjoined claims.

Docket # P8123

CLAIMS

What is claimed is.

1. A method of forming a device comprising:

patterning a first oxide upon a substrate;

forming a first nitride spacer mask upon the first oxide;

forming a first oxide spacer mask upon the first nitride spacer mask;

forming a second nitride spacer mask upon the first oxide spacer mask;

forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask; and

forming a gate layer over the plurality of channels, wherein each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.

2. The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer.

3. The method according to claim 1, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer.

4. The method according to claim 1, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer.

5. The method according to claim 1, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks.

6. The method according to claim 1, wherein forming a first nitride spacer mask comprises:

forming a first nitride layer over the first oxide; and

performing a reactive ion etch upon the first nitride layer, wherein forming a first oxide spacer mask upon the first nitride spacer mask comprises:

forming a first oxide layer over the first nitride spacer mask; and

performing a reactive ion etch upon the first oxide layer, wherein forming a second nitride spacer mask upon the first oxide spacer mask comprises:

forming a second nitride layer over the first oxide spacer mask; and

performing a reactive ion etch upon the second nitride layer, wherein forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask comprises:

performing a gate etch with the second nitride spacer masks, and further comprising: forming a gate oxide upon the plurality of channels.

7. The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 300 nm.

8. The method according to claim 1, wherein the first oxide is patterned with a width of about 100 nm and a pitch of about 320 nm.

9. The method according to claim 1, wherein the substrate is made by providing a silicon on insulator substrate, and wherein the plurality of channels comprises monocrystalline silicon channels.

10. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, and wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels.

11. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, and wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels.

12. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein the trench is filled with a dielectric, and wherein

the plurality of channels comprises a plurality of single-gate quantum wire field effect transistors.

13. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein each of the plurality of channels has a gate oxide layer disposed thereupon, and wherein the second nitride spacer mask is disposed between the channel and the gate layer.

14. The method according to claim 1, wherein the plurality of channels comprises a plurality of triple-gate quantum wire field effect transistors.

15. The method according to claim 1, wherein the substrate comprises monocrystalline silicon, wherein the plurality of channels is spaced apart by a trench that is at least as wide as each of the channels, wherein a doping region is disposed in the substrate beneath the trench that resists electrical communication between adjacent spaced-apart channels, and wherein the substrate is part of a silicon on insulator structure.

16. A method of forming a device comprising:

patterning a first oxide having a first width upon a substrate;

forming a first nitride layer upon the first oxide and the substrate, wherein the first nitride layer has a first thickness that is less than the first width;

forming a first nitride spacer mask from the first nitride layer, wherein the first nitride spacer mask has a width equal to the first nitride layer thickness;

forming an oxide layer upon the first nitride spacer mask, wherein the oxide layer has a second thickness that is less than the width of the first nitride spacer mask;

forming a first oxide spacer mask from the oxide layer, wherein the first oxide spacer mask has a width equal to the first oxide layer thickness;

forming a second nitride layer upon the first oxide spacer mask, wherein the second nitride layer has a thickness that is less than the width of the first oxide spacer mask;

forming a second nitride spacer mask from the second nitride layer;

removing the first oxide spacer mask;

performing an etch over the second nitride spacer mask to form at least one semiconductor channel having a channel width and a length, wherein the mean free electron path therein is larger than the channel width;

forming a dielectric layer upon the channel length; and

forming a gate layer over the channel.

17. The method according to claim 16, wherein the first oxide has a width of X and a pitch of about 3X.

18. The method according to claim 16, wherein each performing a spacer etch comprises performing a reactive ion etch.

19. The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels, wherein each of the plurality of semiconductive channels has a width of about one-tenth X;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

20. The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

removing the patterned second nitride spacer mask;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

21. The method according to claim 16, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

forming an oxide upon the SOI topology;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic width from about 2X to about 10X.

22. A method of forming a device comprising:

patterning a first oxide upon a substrate, wherein the first oxide has a characteristic width of X and a characteristic pitch selected from about 3X and about 3.2X;

forming a first nitride layer upon the oxide, wherein the first nitride layer has a characteristic thickness of about one half X;

performing a spacer etch upon the nitride layer and removing the oxide to form a patterned first nitride spacer mask;

forming an oxide layer upon the patterned first nitride spacer mask, wherein the oxide layer has a characteristic thickness of about one fourth X;

performing a spacer etch upon the oxide layer and removing the patterned first nitride spacer mask to form a patterned first oxide spacer mask;

forming a second nitride layer upon the patterned first oxide spacer mask, wherein the second nitride layer has a characteristic thickness of about one-tenth X; and

performing a spacer etch upon the second nitride layer and removing the first oxide spacer mask to form a patterned second nitride spacer mask.

23. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride spacer mask to form at least one semiconductor channel wherein the mean free electron path therein is larger than about one-tenth X.

24. The method according to claim 22, wherein X is in a range from about 20 nm to about 200 nm.

25. The method according to claim 22, wherein each performing a spacer etch comprises performing an reactive ion etch.

26. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

27. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

removing the patterned second nitride spacer mask;

forming an oxide upon the SOI topology; and

forming a gate layer over the oxide.

28. The method according to claim 22, further comprising:

performing an etch over the patterned second nitride that forms a silicon on oxide (SOI) topology of a plurality of semiconductor channels wherein the mean free electron path in each of the plurality of channels is larger than about one-tenth X;

forming an oxide upon the SOI topology;

forming a gate layer over the oxide; and

forming a contact that connects with the plurality of channels, wherein the contact has a characteristic width from about 2X to about 10X.

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29. A device comprising:

a plurality of semiconductive channels, each of the plurality of semiconductive channels comprising a channel length and a channel width;

a dielectric layer disposed upon the semiconductive channel length;

a source at a first terminal end of the plurality of semiconductive channels, and a second terminal end of the plurality of semiconductive channels;

a gate layer disposed over the dielectric layer, wherein electron flow in the plurality of semiconductive channels has a mean free path that is greater than the semiconductive channel width, and wherein a first semiconductive channel is spaced apart from a second semiconductive channel by a trench that is less than about five times the semiconductive channel width.

30. The device according to claim 29, wherein the plurality of semiconductive channels comprises monocrystalline silicon that is disposed upon a dielectric.

31. The device according to claim 29, wherein the plurality of semiconductive channels comprises monocrystalline silicon that has a self-aligned doping region in the monocrystalline silicon beneath the trench.

32. The device according to claim 29, further comprising:

a mask disposed upon the semiconductive channel width, wherein the device comprises a double-gate quantum wire.

33. The device according to claim 29, wherein the semiconductive channel width is in a range from less than or equal to about 5 nm to about 30 nm.

34. The device according to claim 29, further comprising:

a mask disposed upon the semiconductive channel width, wherein the trench is filled with material comprising the gate layer.

35. The device according to claim 29, wherein the device comprises a triple-gate quantum wire.

36. The device according to claim 29, further comprising:

a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels upon a contact landing pad.

37. The device according to claim 29, further comprising:

a contact that makes electrical connection with one of the terminal ends of the plurality of semiconductive channels, wherein the contact has a characteristic width in a range from about 200 nm to about 1,000 nm.

38. The device according to claim 29, further comprising:

a trench disposed between the first semiconductive channel and the spaced-apart second semiconductive channel, wherein the trench is filled with the dielectric material that is disposed on the semiconductive channel length.

ABSTRACT OF THE INVENTION

The present invention relates to a method of forming a quantum wire gate device. The method includes patterning a first oxide upon a substrate. Preferably the first oxide pattern is precisely and uniformly spaced to maximize quantum wire numbers per unit area. The method continues by forming a first nitride spacer mask upon the first oxide and by forming a first oxide spacer mask upon the first nitride spacer mask. Thereafter, the method continues by forming a second nitride spacer mask upon the first oxide spacer mask and by forming a plurality of channels in the substrate that are aligned to the second nitride spacer mask. A dielectric is formed upon the channel length and the method continues by forming a gate layer over the plurality of channels. Because of the inventive method and the starting scale, each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein.

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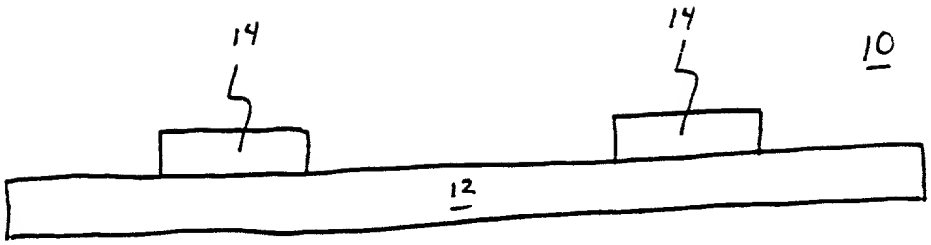

Fig. 1a

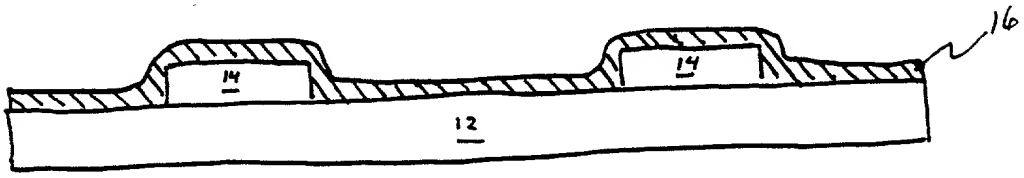

Fig. 1b

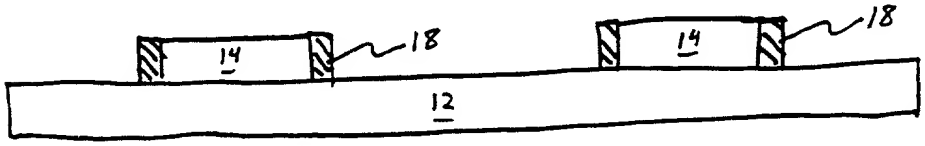

Fig 1c

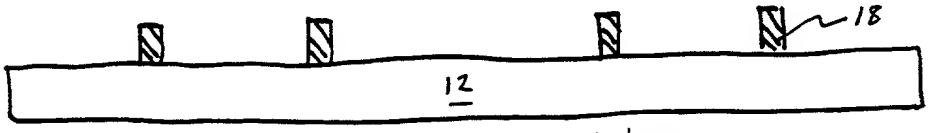

Fig 1d

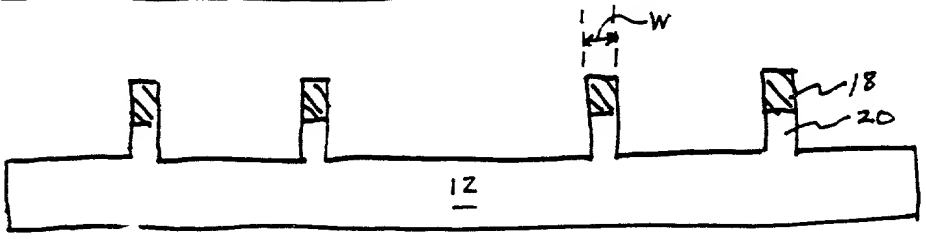

Fig. 1e

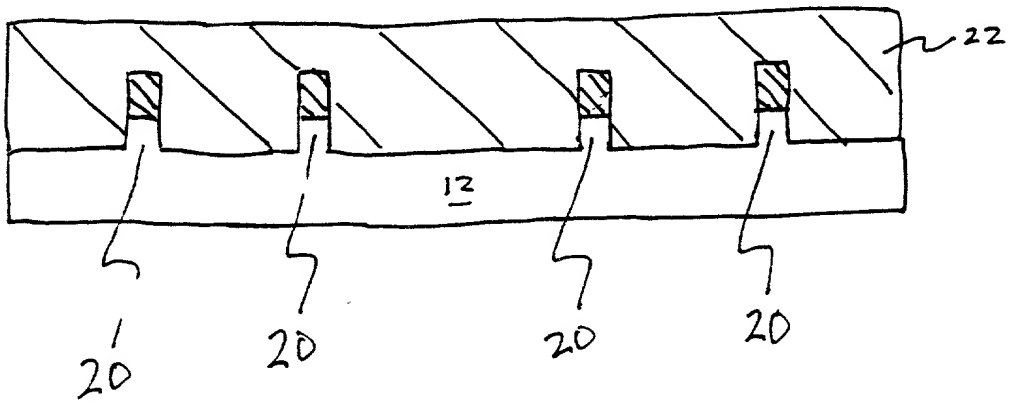

Fig. 1f

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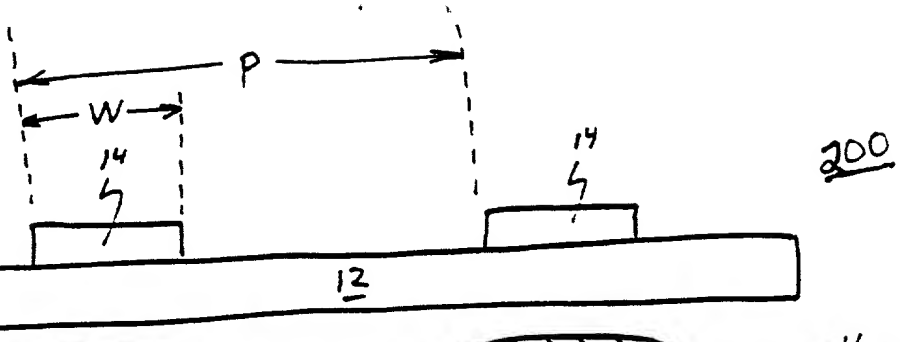

FIG. 2a

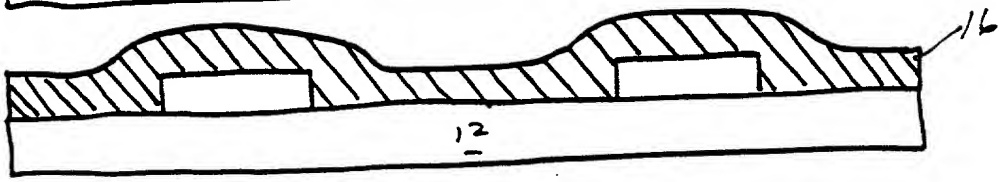

FIG. 2b

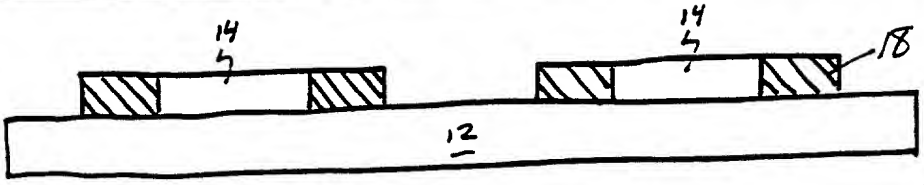

FIG. 2c

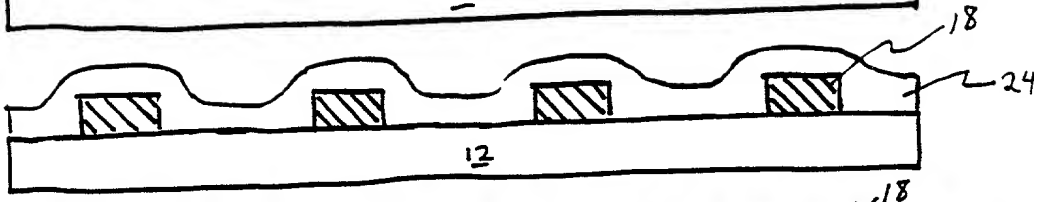

FIG. 2d

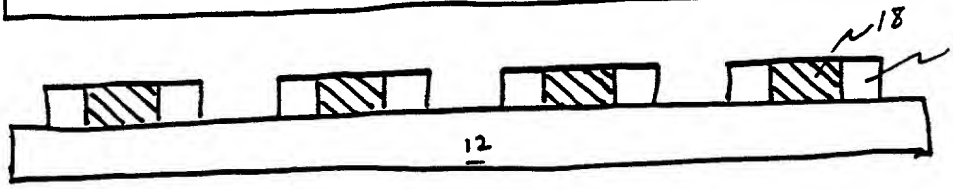

FIG. 2e

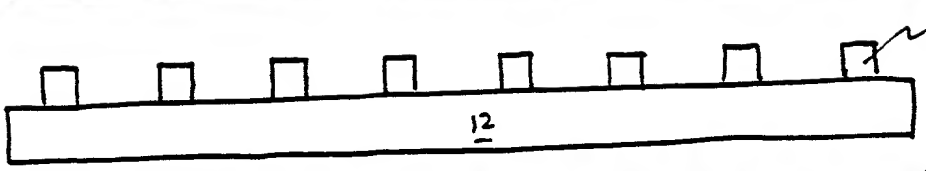

FIG. 2f

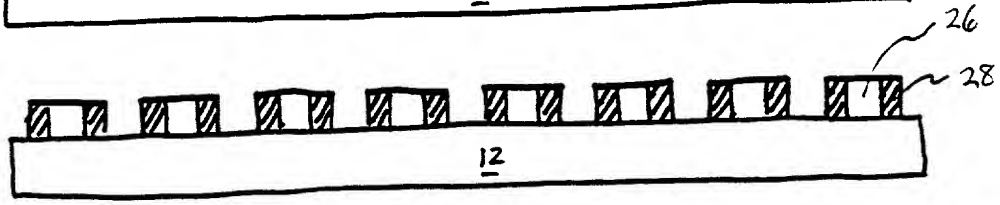

FIG. 2g

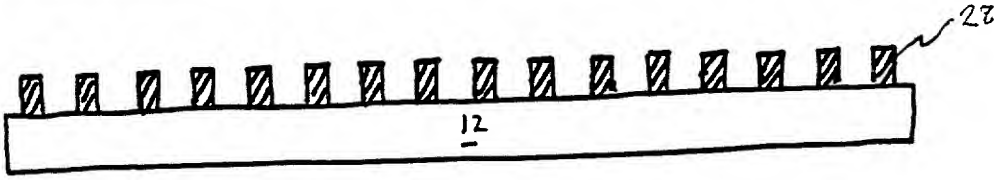

FIG. 2h

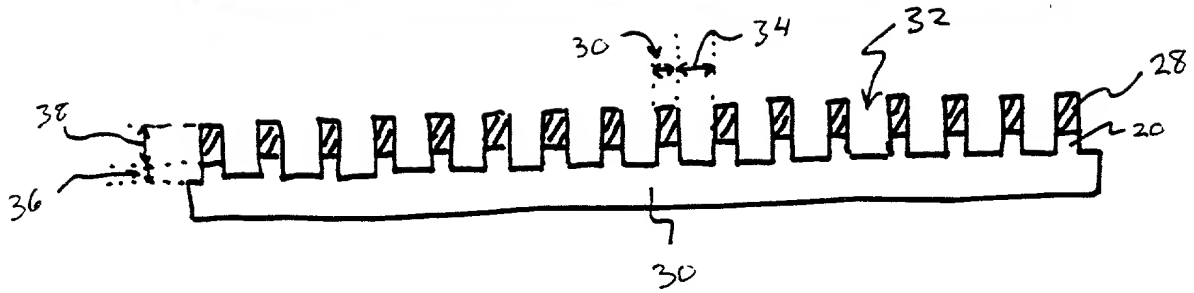

FIG 2i

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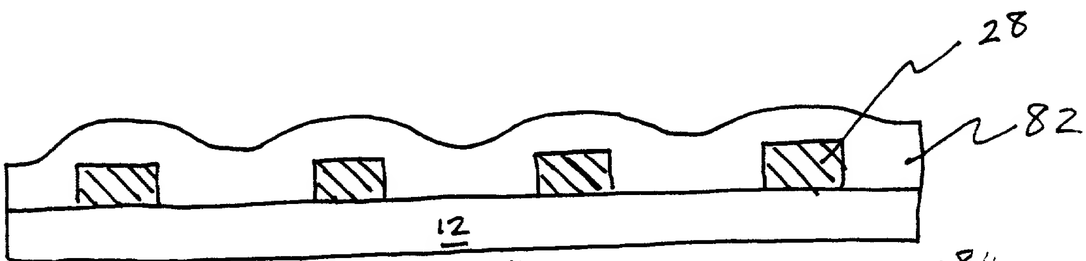


FIG. 3a

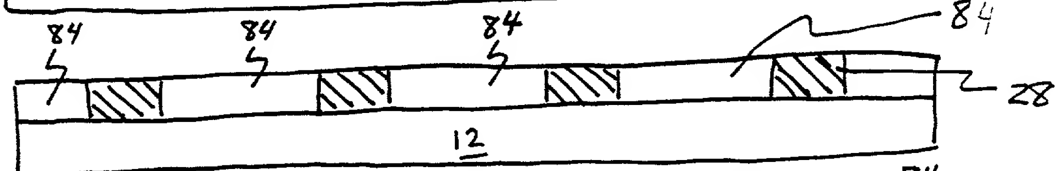


FIG. 3b

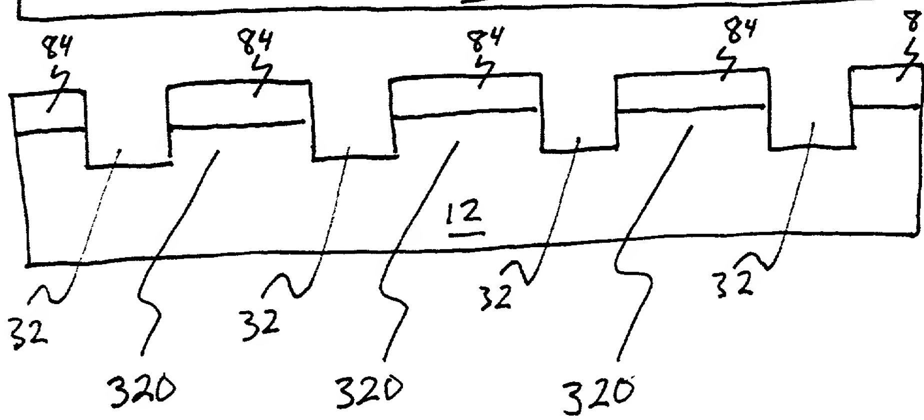


FIG. 3c

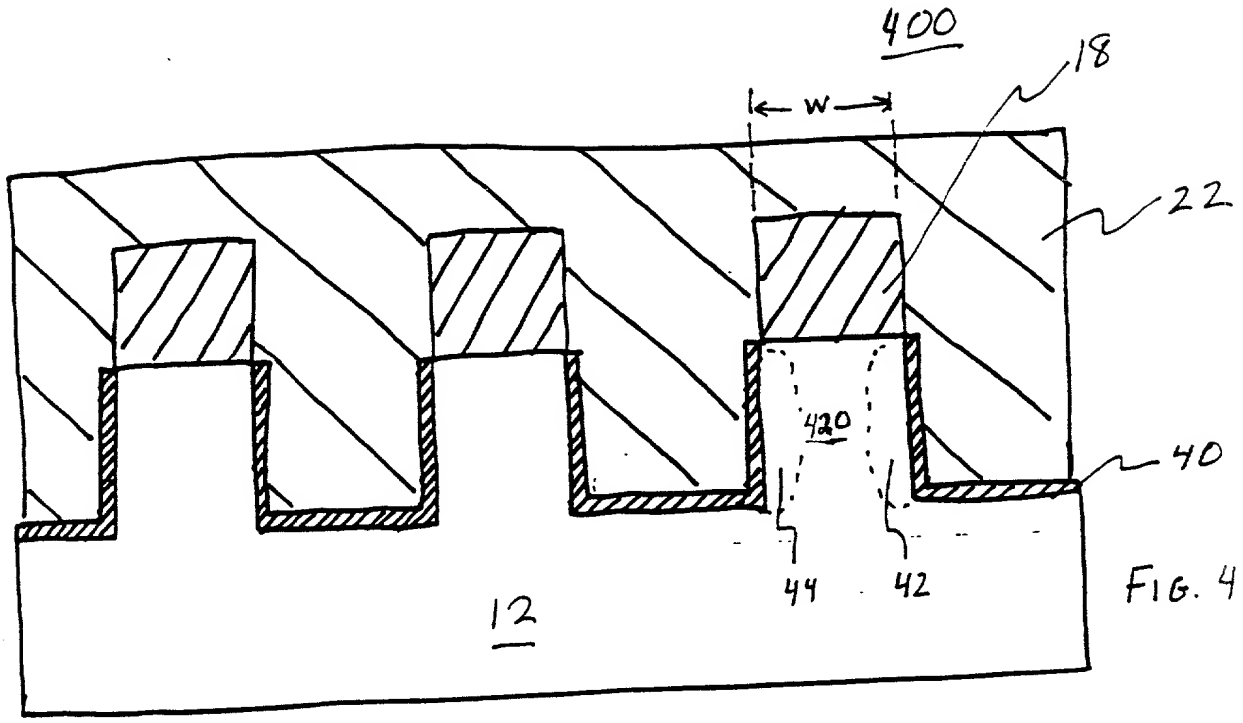


FIG. 4

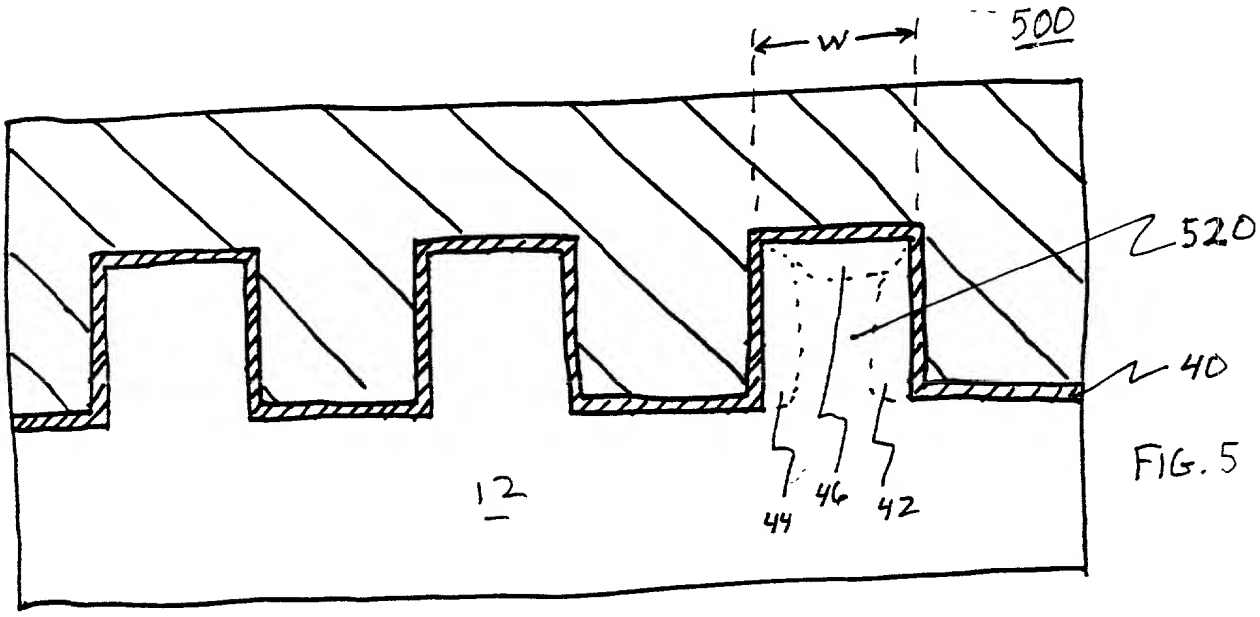


FIG. 5

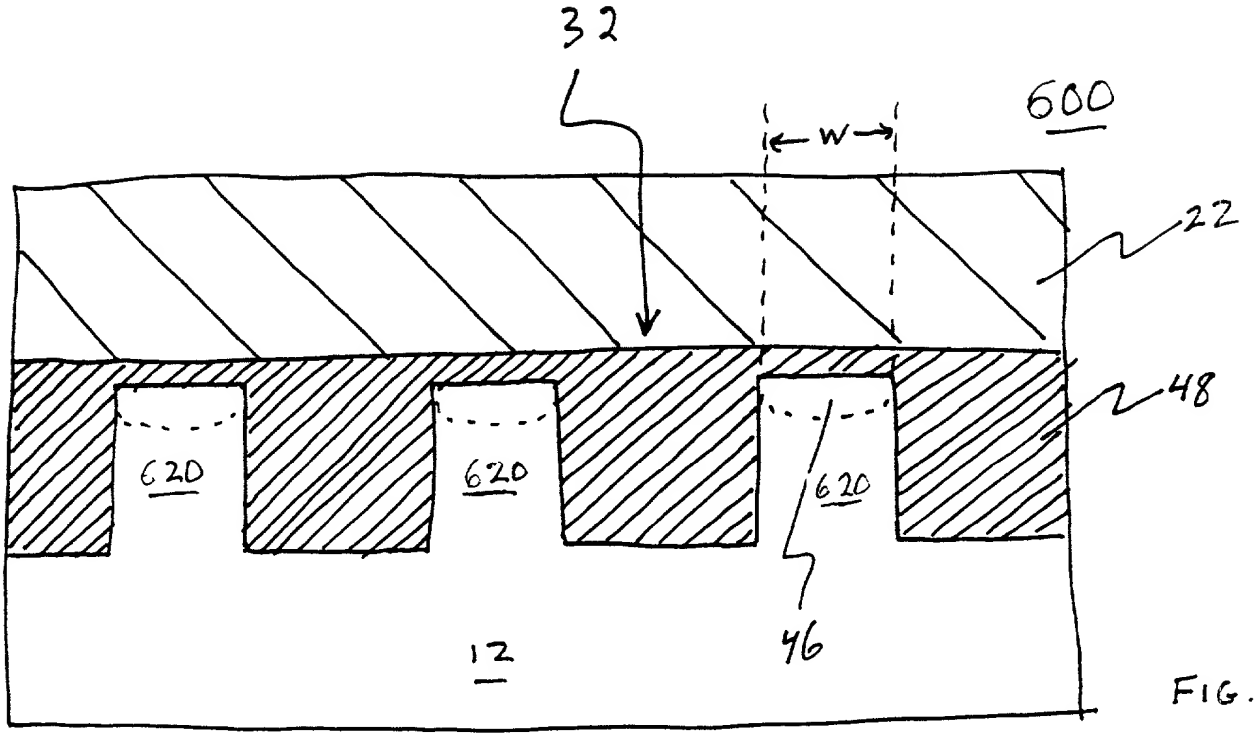


FIG. 6

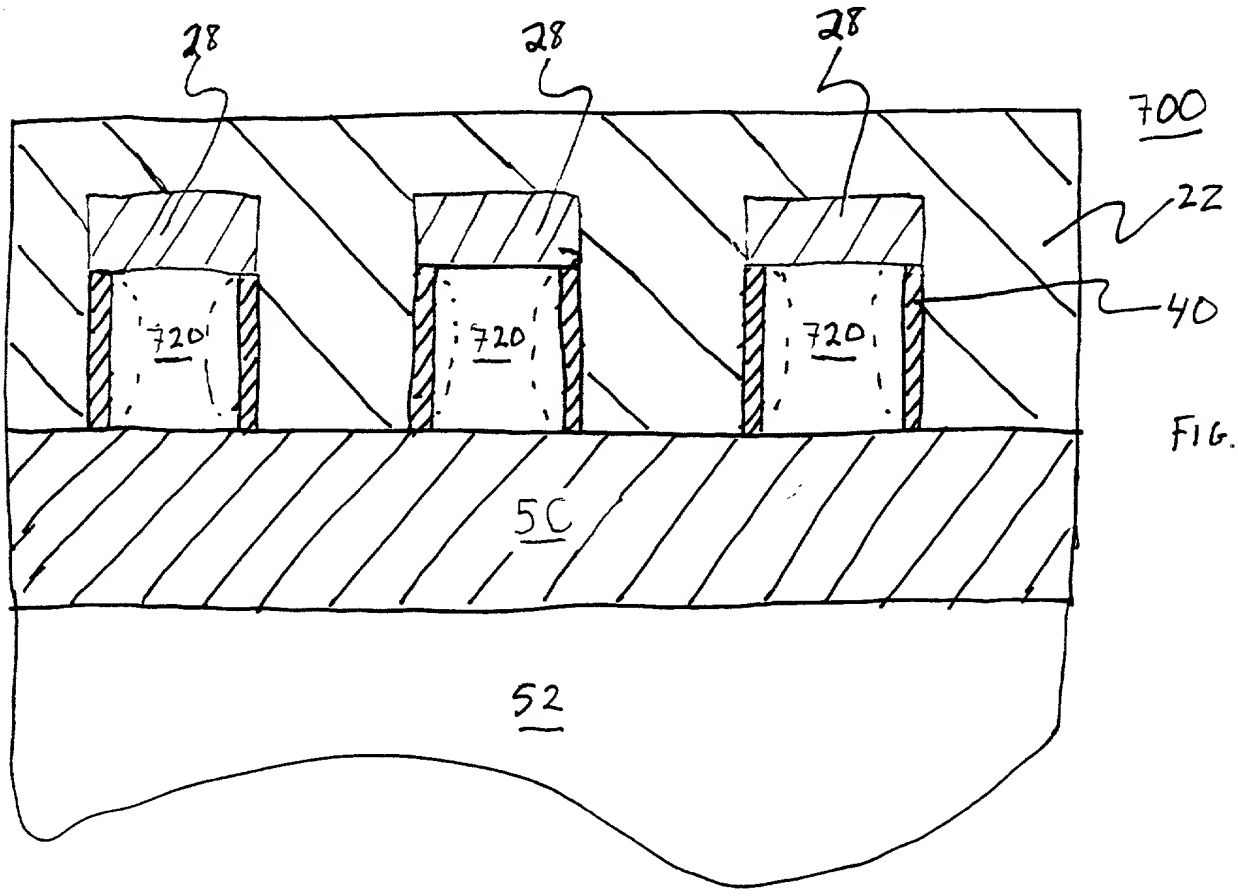


FIG. 7

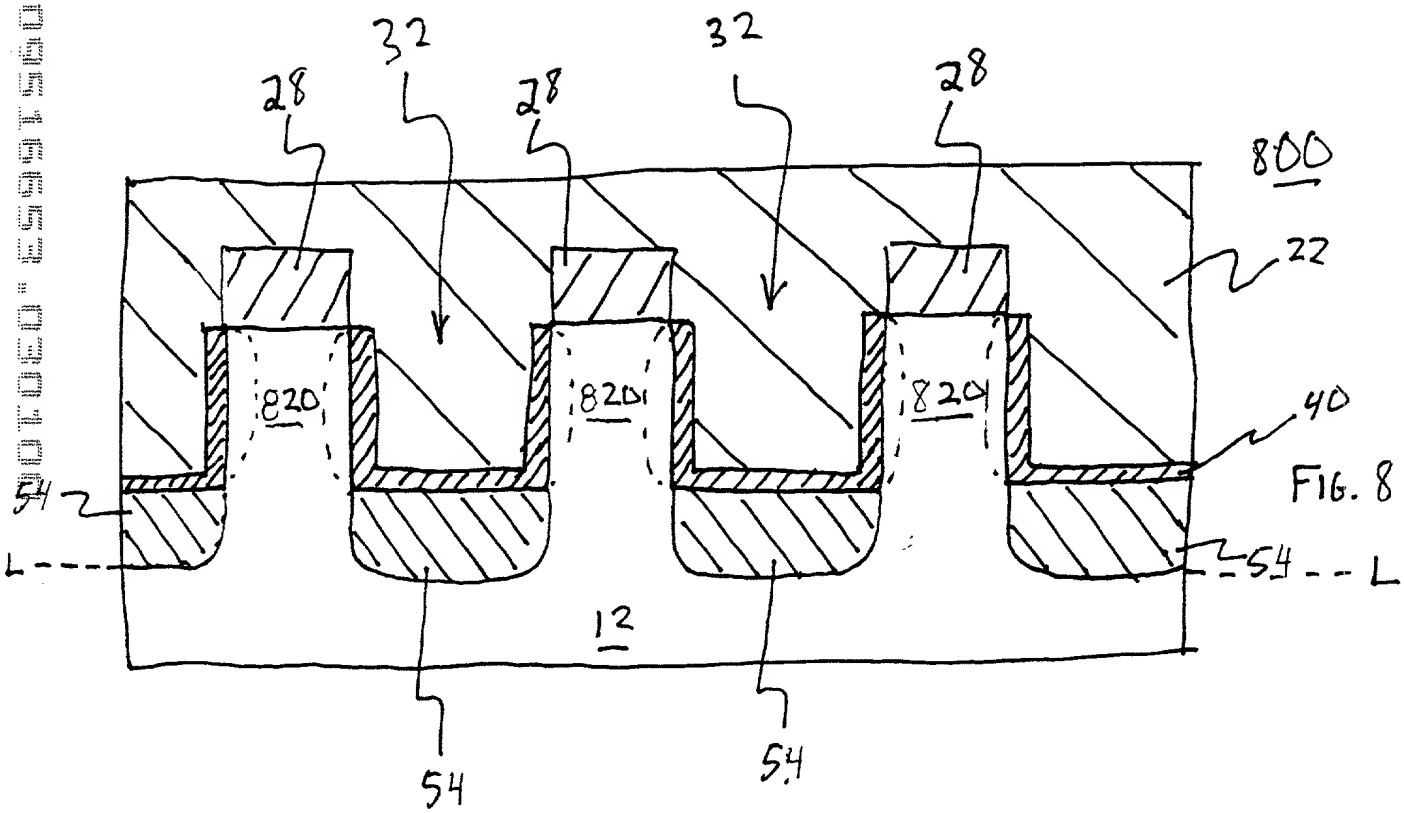


FIG. 8

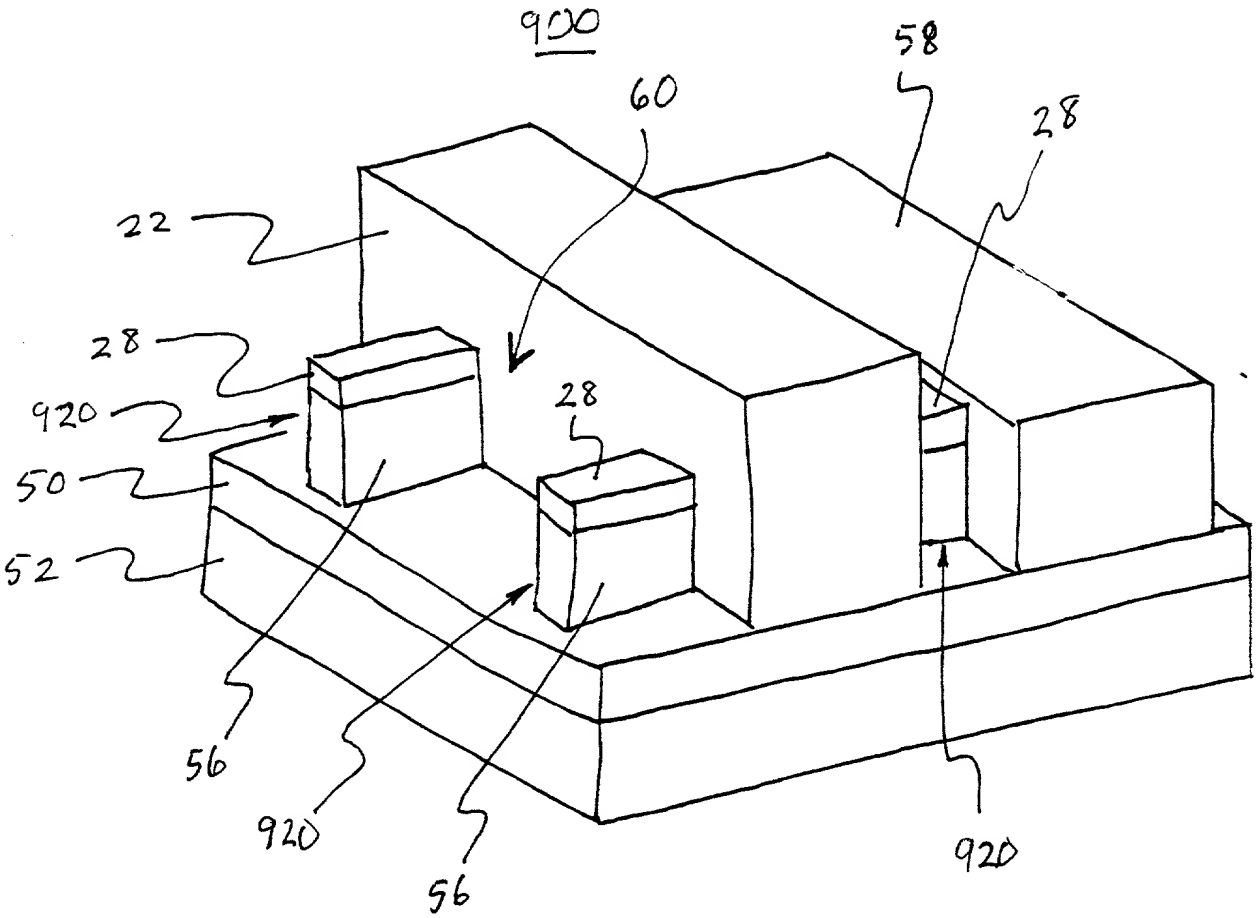
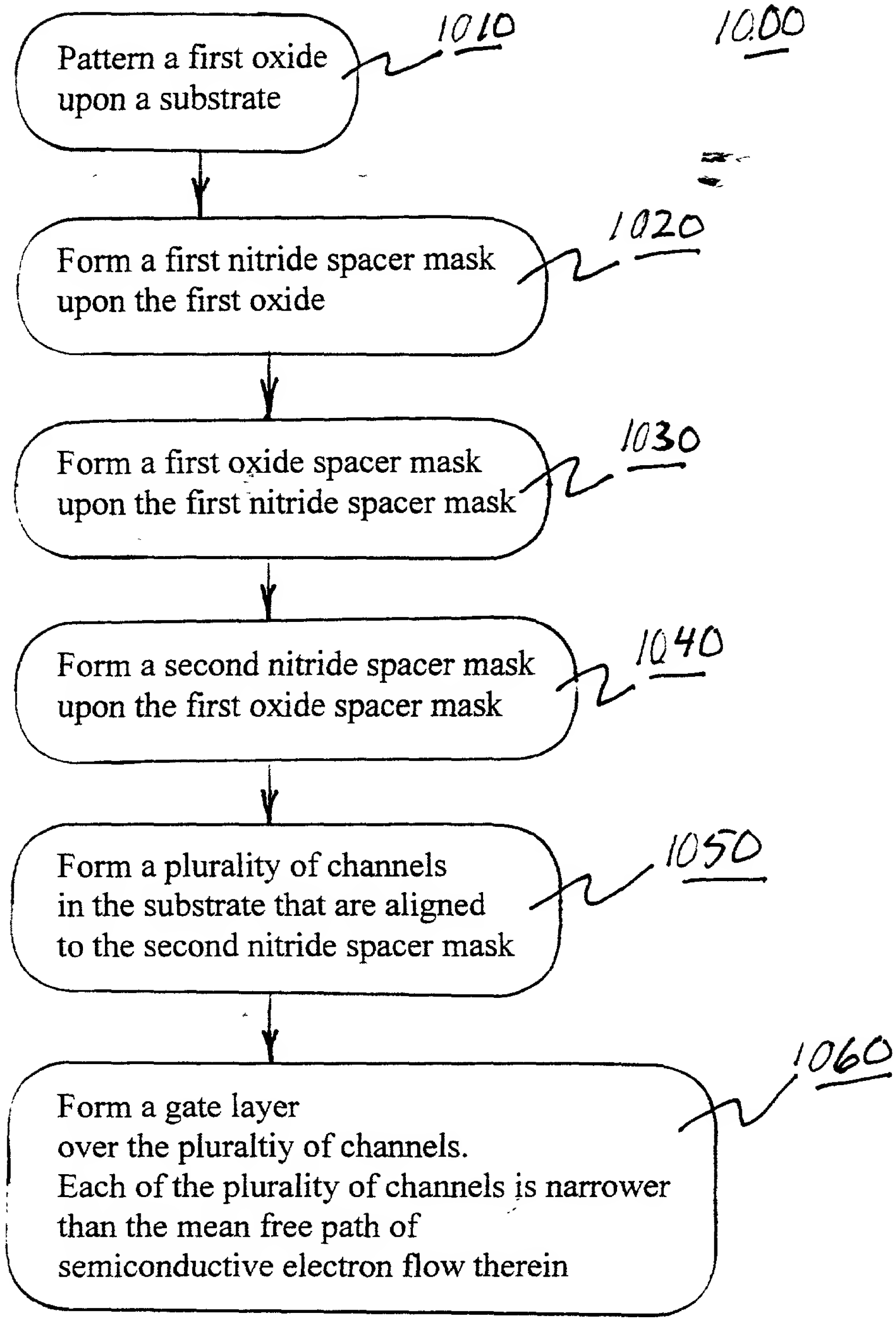


FIG. 9


1000
Pattern a first oxide upon a substrate
1010
Form a first nitride spacer mask upon the first oxide
1020
Form a first oxide spacer mask upon the first nitride spacer mask
1030
Form a second nitride spacer mask upon the first oxide spacer mask
1040
Form a plurality of channels in the substrate that are aligned to the second nitride spacer mask
1050
Form a gate layer over the pluraltiy of channels. Each of the plurality of channels is narrower than the mean free path of semiconductive electron flow therein
1060

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (FOR INTEL CORPORATION PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME

the specification of which

[X] is attached hereto.

[ ] was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

APPLICATION NUMBER	COUNTRY (OR INDICATE IF PCT)	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
			☐ No ☐ Yes
			☐ No ☐ Yes
			☐ No ☐ Yes

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION NUMBER	FILING DATE	STATUS (ISSUED, PENDING, ABANDONED)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to:
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(Name of Attorney or Agent)
12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to:
John N. Greaves, (503) 684-6200.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor (given name, family name) **Brian Doyle**

Inventor's Signature _____ Date _____

Residence Beaverton, Oregon USA (*City, State*) Citizenship Ireland (*Country*)

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APPENDIX A

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